Bias-Engineered Mobility in Advanced FD-SOI MOSFETs

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***Abstract*— Ground-plane (GP) biasing in fully depleted silicon-on-insulator (FD-SOI) MOSFETs allows not only the tuning of the threshold voltage, but also the mobility improvement. We study the carrier mobility enhancement by introducing the return point (or minimum value) of the effective field. This parameter defines the optimum GP bias condition to maximize the mobility gain. Different regions of operation can be discriminated according to the monotonic increase or decrease of the effective field with the front-gate bias. For large mobility enhancement, the return point voltage V_{ret} is adjusted via GP bias such as to exceed the threshold voltage. Experimental results show mobility gains over 70% in SOI MOSFETs with ultrathin buried oxide (10 nm) and Si film (8 nm).**

***Index Terms*— Carrier mobility, effective field, fully depleted silicon-on-insulator (FD-SOI) MOSFETs, ground plane, multibranch mobility, return point, threshold voltage.**

I. Introduction

FULLY Depleted silicon-on-insulator (FD-SOI) technology offers excellent electrostatic control, which translates in better scalability and performance, from low-power to high-speed applications. In planar SOI MOSFETs with thin buried oxide (BOX) and ground-plane (GP), the GP biasing is an effective option for boosting the device characteristics. The GP or back-gate voltage, V_{G2}, is tuned to adjust the threshold voltage in OFF and ON states. But, V_{G2} can also serve for triggering the volume inversion regime, where mobility enhancement was demonstrated [1].

We have recently demonstrated that back-gate biasing leads to unusual, multibranch mobility behavior in FD-SOI MOSFETs and have shown qualitatively that the mobility can sometimes be improved [2]. In this letter, we determine quantitatively the bias regions where the mobility is enhanced or not. Practical guiding rules are given to select the proper bias range for mobility boost. This letter is divided as follows: in Section II, we further investigate the mobility return point concept that reflects the minimum value of the effective field. In Section III, the proposed biasing method is described with experimental data. Multibranch mobility plots will be used to demonstrate the beneficial effects in terms of mobility enhancement.

II. Return Point of Effective Field

The effective field in a MOS transistor, E_{eff}, is defined as the average of the local transverse electric field, $E(z)$, weighted by the local density of inversion carriers, $n_{inv}(z)$, [3]

$$E_{eff}(V_{G1}, V_{G2}) = \frac{\int |E(z, V_{G1}, V_{G2})| n_{inv}(z, V_{G1}, V_{G2}) dz}{\int n_{inv}(z, V_{G1}, V_{G2}) dz} \quad (1)$$

where z corresponds to the transversal direction within the limits of the device channel (Si film in SOI MOSFETs).

A higher field accentuates the carrier confinement at the interface that in turn degrades the mobility. According to the universal mobility curves $\mu(E_{eff})$ [4], the mobility decreases with increasing either the field, the inversion charge or the gate bias. Indeed, in bulk MOSFETs the field always increases with the gate bias. This conventional view is not necessarily true in FD-SOI transistors. While increasing V_{G1}, there is a bias range where the effective field actually decreases hence the mobility improves. Our aim is to exploit this bias window for enhancing the mobility: the ideal case would be to have the electric field decreasing (instead of increasing as usual) for higher values of the gate bias. This situation does not exist in bulk MOSFETs, but can be obtained in FD-SOI MOSFETs via the proper selection of the bias at the front- and back-gates. To understand how this condition can be achieved, we first examine the evolution of the effective field under different biasing conditions. The magnitudes of $E(z)$ and $n(z)$ involved in (1) are not directly accessible from the experiment, thus E_{eff} is evaluated by combining measurements and simulations done with a Poisson–Schrödinger self-consistent solver. We perform Split-C(V) measurements from which the inversion charge is determined, by integration, as a function of the gate bias. Mobility is obtained as $\mu = I_D/(WL/V_D Q_{inv})$, where V_D is the drain voltage used for current measurements [5].

The simulation parameters are fine calibrated to reproduce the experimental $Q_{inv}(V_{G1})$ curves, as shown in Fig. 1(a). The simulation delivers, for each gate bias, the profiles of field $E(z)$ and carrier density $n_{inv}(z)$ that are needed in (1) to calculate E_{eff}. The mobility values shown in this letter are genuinely experimental, the simulations just serve to determine the effective field. This method is recently used to generate

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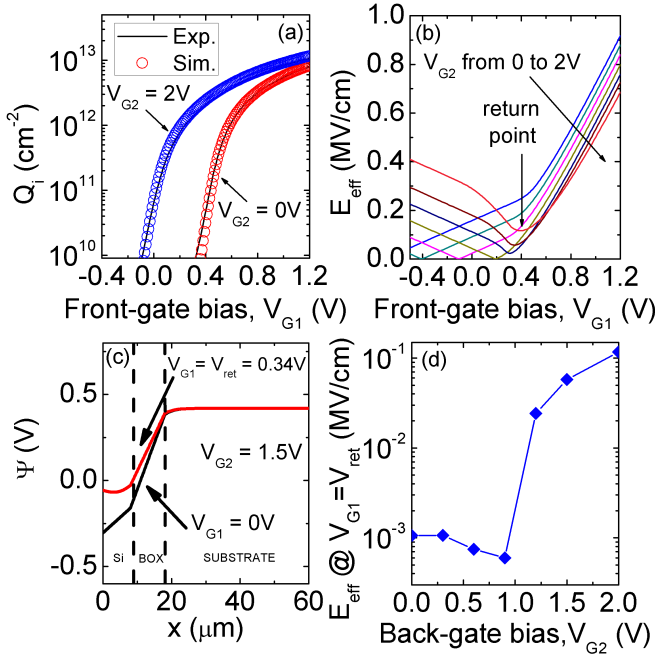

Fig. 1. (a) Comparison of the inversion charge concentration as a function of the front-gate bias between the experimental results (open symbols), calculated by the Split-C(V) technique, and simulation results (solid lines) obtained after the calibration of the solver. Back-gate bias: $V_{G2} = 0$ V and $V_{G2} = 2$ V. (b) Effective field evaluated with (1) versus the front-gate bias for different values of V_{G2} (0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V, 1.5 V, 2 V). For $V_{G2} > 0$ V, two different front-gate biases lead to the same E_{eff} value. (c) Potential cross section for two values of the front-gate bias ($V_{G1} = 0$ V and $V_{G1} = V_{ret} = 0.34$ V) when $V_{G2} = 1.5$ V. (d) Effective field evaluated at the return point as a function of the back-gate bias. $T_{Si} = 8$ nm, $T_{BOX} = 10$ nm, $L = W = 10$ μm, and EOT = 1.3 nm.

unusual, multibranch mobility curves unaccounted by the universal mobility [2], [6]. We now use the same methodology for determining the practical back-gate bias range where the mobility is maximized.

Fig. 1(b) shows the effective field as a function of V_{G1} for different back-gate biases. For positive V_{G2}, there is a range where two different front-gate biases can lead to the same value of effective field. For V_{G1} fixed in strong inversion ($V_{G1} \geq 0.6$ V), a remarkable drop in electric field (by 0.15–0.2 MV/cm) is achieved by turning the back-gate voltage from zero to a modest positive value ($V_{G2} \cong 1.5$ V); this field reduction directly translates in improved mobility (see also Figs. 2(b) and 3(b)). When increasing the front-gate bias the effective field decreases until a minimum point is reached (return point, V_{ret}). Beyond this point ($V_{G1} > V_{ret}$), the field increases monotonically because of the buildup of the front channel. Fig. 1(c) compares the potential profiles at $V_{G1} = 0$ V and $V_{G1} = V_{ret}$ for $V_{G2} = 1.5$ V: the body potential is much flatter at the return point demonstrating the electric field reduction. Fig. 1(d) shows the effective field at the return points that remains moderate even for relatively high back-gate bias. The idea behind our paper is to take advantage of the initial decrease in the effective field. We investigate the bias conditions enabling the transistor to operate in the region where E_{eff} decreases with increasing V_{G1}, hence the mobility will present a remarkable boost.

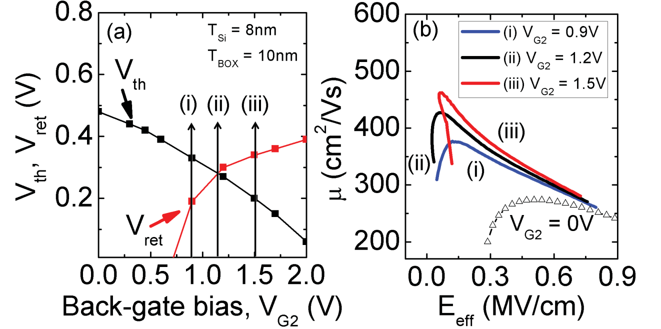

Fig. 2. (a) Bias map of experimental threshold voltage and simulated return point voltage as a function of the back-gate bias. Different regions can be distinguished: *1)* $V_{G2} = 0.9$ V: the transistor reaches the return point before the onset of the channel; *2)* $V_{G2} = 1.2$ V: the threshold voltage and return point are reached simultaneously; and *3)* $V_{G2} = 1.5$ V: the front channel is in strong inversion before the field is minimum. (b) Experimental multibranch curves of mobility versus effective field for the three back-gate biases shown in (a). By comparison, the curve measured for $V_{G2} = 0$ V shows lower mobility. $T_{Si} = 8$ nm, $T_{BOX} = 10$ nm, $L = W = 10$ μm, and EOT = 1.3 nm.

III. Map of Bias Regions

To exemplify our methodology, we selected transistors with ultrathin body and BOX ($T_{Si} = 8$ nm, $T_{BOX} = 10$ nm) fabricated at STMicroelectronics [7]. The optimum bias range for the transistor is defined by two critical parameters, the threshold voltage, V_{th}, and the return point voltage, V_{ret} ($\partial E_{eff}/\partial V_{G1}|_{V_{G1}=V_{ret}} = 0$). The representation of V_{th} and V_{ret} as a function of the back-gate voltage constitutes the bias map shown in Fig. 2(a). The threshold voltage decreases linearly with V_{G2} as established in the Lim–Fossum model [8] for FD-SOI MOSFETs. In contrast, the return point voltage increases with V_{G2} because of the larger electrostatic potential at the back interface.

A higher V_{ret} means a wider bias window where the effective field decreases and the mobility improves with increasing V_{G1}.

We now consider three different bias possibilities for the back-gate shown by arrows in Fig. 2(a).

1) For $V_{G2} = 0.9$ V and increasing V_{G1}, the transistor first reaches the return point ($V_{ret} \approx 0.19$ V) before the threshold voltage ($V_{th} = 0.33$ V). From the return point to the channel activation, the effective field increases. Therefore, the scattering mechanisms are amplified limiting the mobility values as observed in Fig. 2(b).
2) For $V_{G2} = 1.2$ V, the device reaches the threshold voltage and the return point of the effective field simultaneously [$V_{G1} = V_{th} = V_{ret} = 0.28$ V, in Fig. 2(a)]. This means that as soon as the channel is activated, the effective field increases and the mobility drops.
3) More interesting is the case $V_{G2} = 1.5$ V, where the threshold voltage is reached before the return point. The front channel operates in strong inversion before the effective field has attained its minimum value. The consequence is outstanding: increasing the front-gate bias from $V_{G1} = V_{th} = 0.2$ V to $V_{G1} = V_{ret} = 0.34$ V, the effective field is reduced despite the channel being enriched with minority carriers. Only when the return

point is passed ($V_{G1} > V_{ret}$), does the effective field start to increase.

Fig. 2(b) shows mobility curves as a function of the effective field measured for the generic cases 1)–3). The beneficial effect of a positive back-gate bias is evident when comparing these curves with the mobility measured at $V_{G2} = 0$ V. If the back gate is grounded, the mobility is inferior simply because the effective field is much higher, as already noted in Fig. 1(b). Case 3), where $V_{th} < V_{ret}$, is the most favorable for mobility enhancement: the maximum mobility is boosted by a 70% (from 273 cm^2/Vs at $V_{G2} = 0$ V to 462 cm^2/Vs at $V_{G2} = 1.5$ V). The mobility gain decreases as E_{eff} increases and, apparently, all curves merge for $E_{eff} > 0.8$ MV/cm. But, such a critical field is not accommodated for the same V_{G1} voltage. For a given front-gate bias (i.e., $V_{G1} = 1.2$ V) the transistor operates with much reduced effective field ($E_{eff} = 0.73$ MV/cm) at $V_{G2} = 1.5$ V compared with $V_{G2} = 0$ V ($E_{eff} = 0.92$ MV/cm). This difference explains the significant gain in mobility.

The biasing method is also applied to thick-BOX ($T_{BOX} = 145$ nm) transistors fabricated at CEA-LETI [9]. Fig. 3(a) shows the bias map indicating the threshold voltage and return point voltage as a function of V_{G2}. Three back-gate bias conditions are analyzed and compared with the case at $V_{G2} = 0$ V: *1)* $V_{th} > V_{ret}$ for $V_{G2} = 1$ V, *2)* $V_{th} = V_{ret}$ for $V_{G2} = 2$ V, and *3)* $V_{th} < V_{ret}$ for $V_{G2} = 8$ V. The use of the back-gate bias, instead of a grounded substrate, rises the peak mobility by about 10% in cases *1)* and *2)*. It is again the case *3)* where the mobility gain is more pronounced [Fig. 3(b)]: 24% from 376 cm^2/Vs at $V_{G2} = 0$ V to 464 cm^2/Vs at $V_{G2} = 8$ V. The particular knot-like shape of this curve *3)* shows a sharp increase in mobility as the effective field decreases to the minimum value (~ 0.1 MV/cm). The impact of the mobility enhancement is directly visible on the output current and transconductance: for a given gate bias, i.e., $V_{G1} = 0.45$ V, $I_D = 0.64$ μA and $g_m = 6.26$ μS for $V_{G2} = 0$ V, while for $V_{G2} = 8$ V, the gain is significant ($I_D = 1.09$ μA (+70%) and $g_m = 10.60$ μS (+69%)) ultimately leading to improved circuit performance. Similarly, for a given overdrive voltage, i.e., V_{G1}-$V_{th} = 0.8$ V, we measure $I_D = 7.50$ μA and $g_m = 7.81$ μS for $V_{G2} = 0$ V, and for $V_{G2} = 8$ V, $I_D = 8.30$ μA (+9%) and $g_m = 8.66$ μS (+11%). The difference between g_m and mobility gains is due to the shift of g_m peak with V_{G2}.

The bias map representation (combining V_{ret} and V_{th} vs. V_{G2}) is general and allows the selection of the optimal bias condition for the mobility enhancement. This method can, in principle, be implemented for mobility gain in any FD-SOI MOSFETs, but it is best suited in planar ones with thin BOX and GP, where the back-gate voltage can be maintained in the practical 1–2 V range. Furthermore, the bias map can be enriched by adding the benefits of mobility gain and modified values of off-state leakage current and threshold voltage. The combination of these assets is realistic when GP bias is adjusted dynamically to provide high V_T and low leakage in off-state mode and to achieve low V_T, high current and improved mobility in on-state mode.

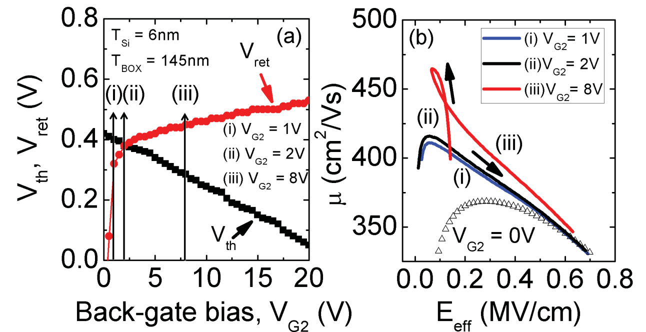

Fig. 3. (a) Experimental threshold voltage and simulated return point voltage versus back-gate bias. Three bias paths are showed: *1)* $V_{G2} = 1$ V, *2)* $V_{G2} = 2$ V, and *3)* $V_{G2} = 8$ V. (b) Corresponding multibranch mobility curves. $T_{Si} = 6$ nm, $T_{BOX} = 145$ nm, $L = W = 10$ μm, and EOT = 1.3 nm.

IV. Conclusion

We introduced the concept of bias-engineered mobility that aimed at operating the transistor in the region of minimum effective field. The return point of the effective field is a convenient tool for the selection and understanding of the optimal bias conditions to enhance the mobility in FD-SOI MOSFETs by using the back-gate bias. The combined representation of the threshold voltage and return point voltage indicated the bias range where the effective field decreases while the front-gate bias is increasing. In this bias window, the mobility was maximized. Our experiments showed a mobility gain of 70% in FD-SOI MOSFETs with 10-nm-thick BOX and GP. Bias engineering of carrier mobility is a simple, pragmatic method that comes together with the V_{th} tunning and can be combined with other types of mobility engineering based on strain, crystal orientation or Si replacement.

References

[1] W. Chaisantikulwat, M. Mouis, G. Ghibaudo, *et al.*, "Experimental evidence of mobility enhancement in short-channel ultra-thin body double-gate MOSFETs by magnetoresistance technique," *Solid State Electron.*, vol. 51, nos. 11–12, pp. 1494–1499, 2007.

[2] C. Navarro, N. Rodriguez, A. Ohata, *et al.*, "Multribranch mobility analysis for the characterization of FDSOI transistors," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1102–1104, Aug. 2012.

[3] M. Shoji and S. Horiguchi, "Electronic structures and phonon limited electron mobility of double-gate silicon-on-insulator Si inversion layers," *J. Appl. Phys.*, vol. 85, no. 5, pp. 2722–2731, 1999.

[4] S. Takagi, A. Toriumi, M. Iwase, *et al.*, "On the universality of inversion-layer mobility in Si MOSFET's: Part I—Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.

[5] A. Ohata, M. Casse, and S. Cristoloveanu, "Front- and back-channel mobility in ultrathin SOI-MOSFETs by front-gate split CV method," *Solid State Electron.*, vol. 51, no. 2, pp. 245–251, 2007.

[6] S. Cristoloveanu, N. Rodriguez, and F. Gamiz, "Why the universal mobility is not," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1327–1333, Jun. 2010.

[7] C. Fenouillet-Beranger, S. Denome, *et al.*, "FDSOI devices with thin BOX and ground plane integration for 32 nm node and below," *Solid State Electron.*, vol. 53, no. 7, pp. 730–734, 2009.

[8] H. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983.

[9] F. Andrieu, O. Weber, J. Mazurier, *et al.*, "Low leakage and low variability ultra-thin body and buried-oxide (UT2B) SOI technology for 20 nm low power CMOS and beyond," in *Proc. Symp. VLSI Technol.*, San Francisco, CA, 2010, pp. 57–58.