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# Effective Capacitance Area for Pseudo-MOSFET Characterization of Bare SOI Wafers by Split-C(V) Measurements

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We have investigated the effective area involved in Split-C(V) measurements performed in Pseudo-MOSFET configuration. This area cannot be directly determined from dimensional relations and must be extracted according to experiments. Firstly, we have examined the variation of this area with the frequency of the AC signal used to generate capacitance curves, and with the configuration parameters of the experimental setup (the number of the needles and the distance between them). A model to evaluate the effective area in any characterization scenario has been proposed and validated with systematic measurements. Finally, we discussed the carrier density determination by using the active area derived from Split-C(V) measurements.
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The Split-C(V) technique has been widely used to obtain the inversion or accumulation charge from the integration of the gate-to-channel capacitance curve in MOSFETs.[1,2] However, this characterization technique has still to address some points related to the effective area when it is applied to a Pseudo-MOS transistor.[3] On one hand, the transistor area (active region) is not physically defined by a gate rectangle,[4] unlike the conventional MOSFET. On the other hand, the distance between the needles and the size of the silicon island play an important role due to border effects: when the effective area becomes comparable to the cell size, the electric field distribution in a finite Si cell is different from that of a borderless case.[5]

This paper has been organized as follows. In Section I, we introduce the basics of the Split-C(V) measurements in the Pseudo-MOSFET configuration. In Section II, we show experimental results obtained under different measurement conditions (i.e. changing the frequency and probe pressure or illuminating the wafer). In Section III, we define the active area and comparing and discussing the data obtained experimentally and calculated by the proposed model. Finally, in Section IV we evaluate the carrier density in the channel calculated from capacitance curves and validate the results with numerical simulations.

### Capacitance Measurements by Split-C(V) Method

The Pseudo-MOSFET technique has served during decades for the fast monitoring of SOI wafers by allowing the application of standard extraction methods due to its intrinsic upside-down MOS configuration.[3] Its success relies on its simplicity: as shown in Figure 1a, the substrate of the wafer can be biased ($V_{SUB}$) acting as a gate together with the Buried Oxide (BOX). To complete the transistor, two metallic needles are placed on the surface of the wafer acting as source and drain. A recent expansion of this technique employs the Split-C(V) method to extract the carrier density through capacitance measurements.[4]

The schematic of the experimental setup to obtain the gate-to-channel capacitance curves as well as the equivalent impedance model for the structure are illustrated in Figures 1b and 1c, respectively. For the electrical measurements, we used an Agilent 4294A impedance analyzer with a series Rs-Cs impedance model (suppressing the dispersive effect of the series resistance in the curves). The low potential probe of the impedance analyzer was connected to the needle in direct contact with the channel, and the high potential one was connected to the gate (wafer substrate). The needle pressure was controlled by pressure-adjustable probe arms. A parallel resistance in the BOX was not considered due to the extremely low leakage currents in the thick BOX of the samples ($T_{BOX}$ = 145 nm). The experiments were carried out in MESA-isolated square islands of 5 mm × 5 mm of a 88 nm-thick Si film non-intentionally doped ($N_A \approx 10^{14}$ cm$^{-3}$) non-passivated[6] SOI wafer.

Figure 2a shows the maximum capacitance values, $C_{max}$, extracted from C-V curves obtained from the experimental configuration of Figure 1b (one single needle on the surface of the cell). The oscillation level of the signal was *20 mV* and the frequency was modified from *300 Hz* to *100 kHz*. Two different behaviors are manifested: for frequencies below *1 kHz*, $C_{max}$ is saturated for both hole and electron channels (what is translated in symmetrical capacitance curves for holes and electrons in Figure 2a inset). In the region between the threshold voltages for holes and electrons channels, the capacitance is close to zero, demonstrating that the Si film of our samples behaves as fully depleted. The results guarantee the validity of the Split-C(V) technique in the Pseudo-MOSFET since, under FD conditions, only the electrons (or holes) that form the channel are detected in the measurements. At higher frequencies, $C_{max}$ decreases, being this reduction more marked for holes (leading to asymmetrical curves). This frequency dependence occurs due to the under-reaction of the carriers that form the channel in the Si film to follow the potential changes caused by the AC signal. The direct consequence is a clear decrease of the effective area, $S_{eff}$, defined as the region where the carriers (electrons or holes depending on the substrate bias) are participating in the strong inversion or accumulation during capacitance measurements. This fact was verified by performing C-V curves when the wafer was illuminated with a wide-spectrum light. Figure 2b shows the curves obtained by illuminating the cell surface at *280* lux and using an AC frequency of *5 kHz*. As observed, the p-type side of the curve ($V_{SUB} < 0\,V$) is recovered by stimulating the generation of holes (in comparison with the curve obtained in dark condition).

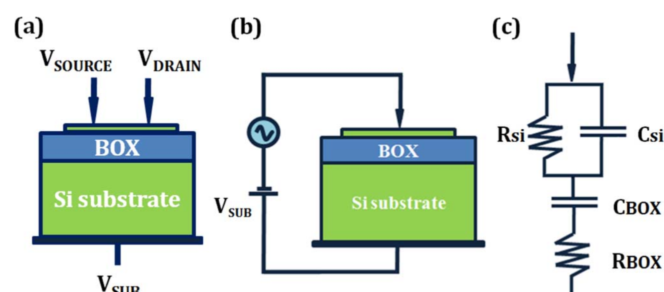


**Figure 1.** (a) Schematic configuration of a Pseudo-MOSFET, (b) combination of the Pseudo-MOSFET method with Split-C(V) technique, and (c) the general impedance equivalent model.

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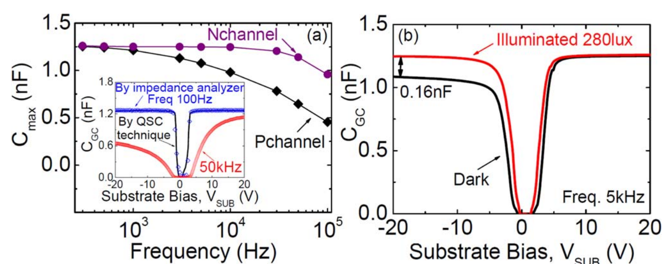


**Figure 2.** (a) Maximum values of the gate-to-channel capacitance curves as a function of the AC signal frequency for both hole and electron channels when the frequency is modified from 300 Hz to 100 kHz in a one-needle configuration. The inset figure compares the capacitance curves obtained from quasi-static capacitance measurements (line) and from the impedance analyzer at 300 Hz and 50 kHz (symbols). (b) Variation of the capacitance curve with or without illumination on the wafer. Non-passivated SOI wafer, $T_{Si} = 88$ nm, $T_{BOX} = 145$ nm.

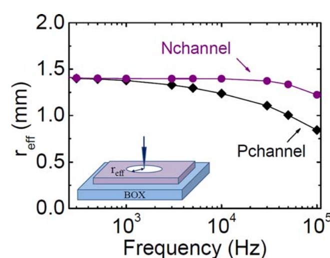


**Figure 4.** Effective radius extracted from capacitance curves used for Figure 2a. The inset shows an schematic representation of the area covered by the carriers in a single-needle configuration.

In order to confirm the validity of the data in terms of saturation of the capacitance at low frequency, quasi-static capacitance measurements[7] (QSC), were performed. The inset in Figure 2a shows the comparison of the C-V measurements obtained by QSC method and those produced by using the impedance analyzer at *100 Hz*. The agreement of both curves demonstrates that, for frequencies below *100 Hz*, the capacitance in the Pseudo-MOSFETs remains saturated, i.e. the carriers have covered the maximum surface according to the potential distribution and the silicon island dimensions. Another curve obtained at *50 kHz* was added to demonstrate the limited response of the carriers to the AC signal.

It was reported previously that the pressure of the needles over the wafer surface causes a noticeable difference in the current driven by the Pseudo-MOSFET.[5] We further studied the impact of this experimental parameter on the C-V curves. Figure 3 shows the dependence with the pressure of the needles on the maximum value of the capacitance and on the threshold voltage for hole and electron channels ($V_{TH-H}$ and $V_{TH-E}$, respectively) both determined by the peak of the second derivative on the capacitance curves. The results show that $V_{TH-H}$ and $V_{TH-E}$ remain constant regardless the probe pressure. The same behavior occurs with $C_{max}$: the values increase very slightly for higher pressures (less than *5.4%*).

In is worth mentioning that if the pressure on the needles is very low (the minimum value possible with our experimental setup is about *5 gr*), the resistance of the film, $R_{Si}$ in Figure 1c, should be taken into account being the total impedance[8] in this case as:

$$Z = 1/j\omega C_{BOX}\cdot(1+j\omega R_{Si}(C_{BOX}+C_{Si}))/(1+j\omega R_{Si}C_{Si})+R_{BOX} \quad [1]$$

Nevertheless, the pressure used was high enough (*>60 gr*) to decrease $R_{Si}$ turning the total impedance given by Eq. 1 into a $R_{BOX}$-$C_{BOX}$ series model, where the maximum value of the capacitance corresponds to the BOX capacitance. This is the reason why the Pseudo-MOSFET is assumed as a series impedance model in our measurements. Pressures higher than *70 gr* were avoided in order not to cause unnecessary damages to the wafer.

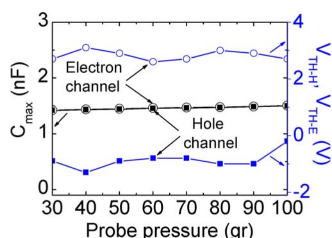


**Figure 3.** Maximum capacitance values at 100 Hz and threshold voltages obtained as a function of the probe pressure in a two-needle configuration. Non-passivated SOI wafer, $T_{Si} = 88$ nm, $T_{BOX} = 145$ nm.

### Single-Needle and Multiple-Needle Effective Surface

For the conventional MOS transistors, the dimensions of the effective area during Split-C(V) measurements are given by the mask size. Nevertheless, this situation is different in a Pseudo-MOSFET since $S_{eff}$ is not physically defined by the gate rectangle and it must be determined experimentally. The simplest formula which allows to relate $S_{eff}$ with the gate-to-channel capacitance, $C_{GC}$, assumes that for thick enough BOX wafers, $C_{GC}$ matches with the BOX capacitance, $C_{BOX}$:

$$C_{GC} \approx C_{BOX} = S_{eff}\,\varepsilon_{BOX}/t_{BOX} \quad [2]$$

This approximation is reasonable for thick-BOX SOI wafers since the substrate effect can be neglected.[4] If we assume that the silicon island is large enough, so border effect can be ignored, the effective surface generated by one needle can be modeled by a circular shape: carriers are uniformly distributed around the needle covering a circular area (Figure 4a). In that case, the area can be estimated by:

$$S_{eff-1N} = \pi r_{eff}^2 \quad [3]$$

The effective radius, $r_{eff}$, is a key value which will account for the dependence of the area on the frequency. Using the same sample of Section I, $r_{eff}$ is approximately *1.4 mm* at low frequencies as shown in Figure 4, being smaller than the dimensions of the cell ($d_{cell} = 5$ *mm*) and comparable to the nearest distance between two needles ($d = 1.59$ *mm*).

When two needles are used for the measurements, the area will be the total surface covered by the two circular regions:

$$S_{eff-2N} = 2\pi {r_{eff}}^2 \quad [4]$$

Nevertheless, there are two aspects to take into account in this first approach. First, when two needles are employed, it is possible that an overlap of the circles occurs for specific frequencies. The overlapped region (named *A* in Figure 5a) is calculated with Eq. 5 and must be subtracted twice from the expression given by Eq. 4. This term is not always necessary, so we define a parameter, $k_1$, to be *1* when overlap

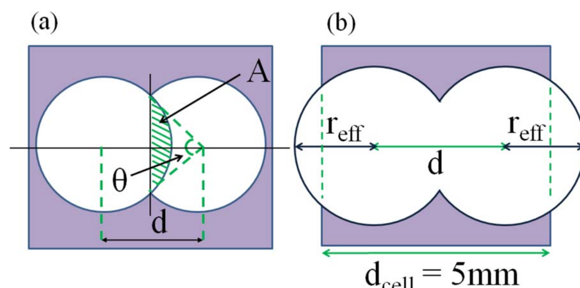


**Figure 5.** Schematics illustrating the definition of the effective surface, $S_{eff}$, for two needles placed on the surface. (a) When an overlap occurs, the region *A* must be subtracted twice from the effective surface. (b) The physical boundaries of the etched silicon island limit the effective surface for large needle separation.

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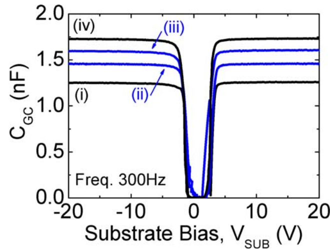


**Figure 6.** Experimental capacitance characteristics with: case (i), one needle on the surface; case (ii) two needles on the surface separated d = 1.59 mm and case (iii) d = 3.18 mm; case (iv) three needles separated d = 1.59 mm. Non-passivated SOI wafer, $T_{Si} = 88$ nm, $T_{BOX} = 145$ nm.

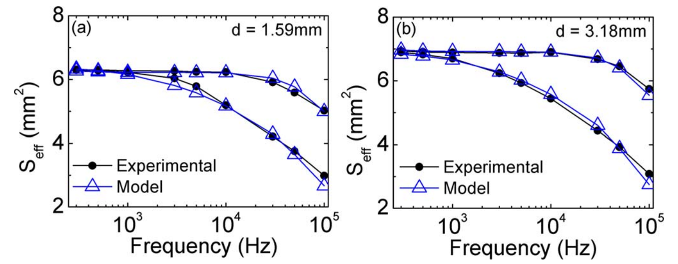


**Figure 8.** Comparison between the effective surface obtained in two-needle configuration extracted with Eq. 2 from experiments (filled dots) and the model proposed in Eq. 8 (open symbols). Both p-Channel and n-Channel are considered. Distance between probes: (a) d = 1.59 mm, (b) d = 3.18 mm. Non-passivated SOI wafer, $T_{Si} = 88$ nm, $T_{BOX} = 145$ nm.

occurs (*$d < 2r_{eff}$*) and *0* for non-overlap, being *d* the distance between the needles.

$$A = 1/2r_{eff}^2[2\arccos(d/2r_{eff}) - \sin(2\arccos(d/2r_{eff}))] \quad [5]$$

Additionally, when the separation between the needles increases and the probes are closer to the edges, it is necessary to define a fitting parameter (α) which takes into account the border effects. The expression of α (Eqs. 6 and 7) was obtained fitting the geometrical relationships from Figure 5b with experimental results. Another constant $k_2$ will determine when the border effects affect the effective area. Its value depends on the physical dimensions of the cell: $k_2$ will be *0* when $d_{cell}$ - $d < 2r_{eff}$ and *1* otherwise. Finally, the expression for the effective surface in a two-needle configuration is shown in Eq. (8).

$$\alpha = (1/\sqrt{2})[1 - k_2(\gamma - \sin\gamma)/(2\pi - k_1(2\arccos(d/2r_{eff}) - \sin(2\arccos(d/2r_{eff}))))] \quad [6]$$

$$\gamma = 2\arccos(d_{cell} - d/2r_{eff}) \quad [7]$$

$$S_{eff-2N} = \alpha(2\pi r_{eff}^2 - 2k_1A) \quad [8]$$

Once we have introduced the effective area term and described a model to obtain it, a set of experiments were performed for validation. Figure 6 shows the capacitance curves measured at *300 Hz* with one, two and three needles on the surface by selecting two different distances between needles. The maximum of the capacitance by two-needle measurements (cases *(ii)-(iii)*) is not twice as large as that by one-needle configuration (case *(i)*) due to the overlapping between areas in each needle and the impact of the border effects. As predicted by the model, when the distance gets larger, so does the capacitance and consequently the effective area.

In order to clarify the different possible situations, Figure 7a shows the theoretical results for the $S_{eff}$ as a function of the distance between the needles calculated using the model given by Eq. 8. The frequency studied was *5 kHz*. As observed, the effective area increases initially with the distance as a consequence of a reduction of the overlapped region. Then, a maximum value is achieved and, for longer distances, the area decreases due to the limits imposed by the size edges of the silicon island. In this context, Figure 7b illustrates an example of the frequency dependence of $S_{eff}$ versus the distance between the probes, *d*, in a hole channel. Concerning the curve at *100 Hz*, the area increases at long distances at the expense of the reduction of the overlapped regions *A*. The maximum value of the effective area is achieved at *2.5 mm* approximately. This peak reflects the distance at which border effects start to affect the $S_{eff}$ since at longer distances, the area starts to decrease. Regarding the remaining curves, when the frequency rises, a plateau region is observed in the curves instead of a peak: the surface covered by each needle results so small that the maximum $S_{eff}$ obtained (before the border effects begin to have influence on it) is the sum of the areas induced by each needle.

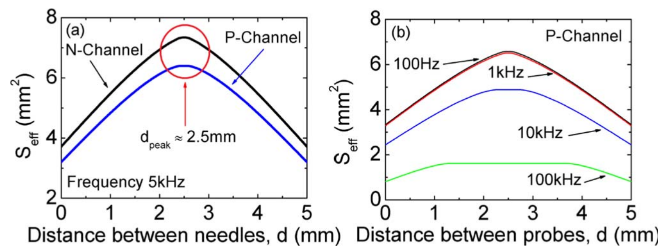


**Figure 7.** (a) Effective area calculated using Matlab software with the model proposed in Eq. 8. $S_{eff}$ increases and decreases depending on the influence of the overlapped and edge regions ($d_{cell} = 5$ mm). (b) Effective surface simulated with the model proposed in Eq. 8 considering several frequencies. If the frequency is high enough, the maximum value of $S_{eff}$ will be the sum of the areas generated by each probe.

Figure 8a shows the comparison between the $S_{eff}$ results obtained experimentally and calculated using the model (Eq. 8) for hole and electron channels when the distance between needles was *1.59 mm*. To determine $S_{eff}$ by the model, we first performed capacitance measurements using only one needle on the surface to calculate the experimental effective radius from the maximum capacitance values. Then, $S_{eff}$ was calculated theoretically by Eq. 8. On the other hand, to obtain $S_{eff}$ experimentally, new capacitance measurements were carried out using two needles on the surface and Eq. 2 was used with the maximum value of them. The results confirm the validity of the model since the agreement between data is good enough in all cases. The same comparison was done for another distance between the needles (*d = 3.18 mm*, Figure 8b) verifying again the model. The fitting between results clarifies that the capacitance decrease observed in Figure 2a is due to the carrier spreading because the theoretical model principles are based on the limited response of electrons and holes to the AC signal.

Finally, Eq. 8 can easily be extended for an arbitrary number of needles aligned on the wafer surface. This expansion of the model requires accounting for the number of needles (*N*) used in the measurements and the number of overlapped regions *A*. The general equation is:

$$S_{eff-N} = \alpha(N\pi r_{eff}^2 - 2(N-1)k_1A) \quad [9]$$

Figure 9 shows the results obtained by performing measurements for an electron channel using three needles on the surface as illustrated in the inset of the Figure and calculated by Eq. 9. The model is validated again; the values predicted fit perfectly with the experiment at low frequencies although an slight deviation is observed at frequencies higher than *20 kHz* (less than *7%*). This deviation may be produced by the difficulty of the linear model to catch the physics of

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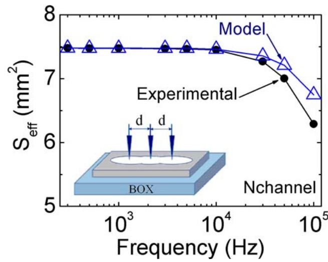


**Figure 9.** Effective surface in a three-needle configuration obtained by using Eq. 2 (circles) and the model proposed in Eq. 9. Non-passivated SOI wafer, $T_{Si}$ = 88 nm, $T_{BOX}$ = 145 nm. The schematic of the experimental setup is shown in the inset.

the potential distribution in the Si film when more than two needles are used.

## Carrier Density Determination

The accumulation or inversion charge, $Q$, in a Pseudo-MOSFET can be determined directly from experimental data using the Split-C(V) method. For example, $Q$ for electrons is calculated by the integration of capacitance curves between $(V_{TH} + V_{FB})/2 \approx 0\ V$ to $V_{SUB}$:

$$Q(V_{SUB}) = \int_0^{V_{sub}} C_{GC} dV_{SUB} \quad [10]$$

Figure 10a depicts the charge calculated by Eq. 10 as a function of $V_{SUB}$ at three different low frequencies using the one-needle configuration shown in Figure 1b. As described previously, at high values of $V_{SUB}$, the maximum of $C_{GC}$ remains saturated without dispersion, leading to a constant value of $S_{eff}$. At these frequencies, due to the lack of frequency dispersion, this area can be also taken as a good approximation for lower $V_{SUB}$ values (always higher than the threshold voltage). In fact, the inset in Figure 10 compares $Q$ obtained by integrating $C_{GC}$ (symbols) by Eq. 10 with a linear fitting (line) of this charge at high values of $V_{SUB}$ (where $C_{max}$ does not vary, $V_{SUB}$ from $15\ V$ to $20\ V$). The agreement is good enough to suggest that the $S_{eff}$ has a constant value between low and high $V_{SUB}$ when the channel is active.

Figure 10b shows the comparison between the inversion charge calculated by integration at $300\ Hz$ using the $C_{GC}$ obtained placing one needle on the surface (line) and using two needles separated $d = 1.59\ mm$ (symbols). For clearer comparison, the capacitance values used for calculations in two-probe configuration, $C_{2N}$, were converted to $C_{2N} \times C_{max1N}/C_{max2N}$ by using the maximum capacitance values obtained in one-needle and two-needle configurations ($C_{max1N} = 1.25nF$ and $C_{max2N} = 1.45nF$). As observed, both curves generate similar results for the whole range of $V_{SUB}$. It demonstrates that, at low frequencies, $S_{eff}$ does not depend on $V_{SUB}$ since the regions $A$ remain constant once $V_{SUB}$ exceeds the threshold voltage.

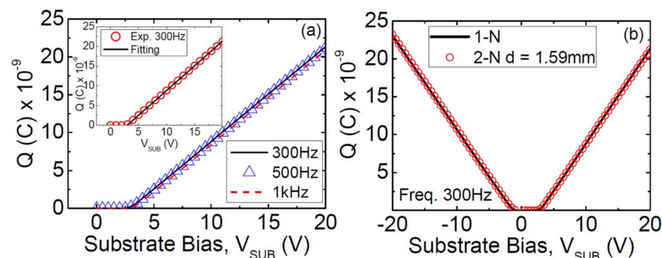


**Figure 10.** (a) Frequency dependence of $Q = \int C_{GC} dV_{SUB}$ with the substrate bias. The difference of Q between 300 Hz and 1 kHz is within 2.1%. The inset figure shows the experimental data of Q and the linear fitting extrapolated from the region between $V_{SUB}$ = 15 V and $V_{SUB}$ = 20 V. This inset results show that even if $S_{eff}$ is determined by $C_{max}$, $S_{eff}$ does not change at low $V_{SUB}$. (b) $Q = \int C_{GC} dV_{SUB}$ for one-needle and two-needle configurations (using d = 1.59 mm as a distance between probes in the second case). For two needles, capacitance values $C_{2N}$ are converted to $C_{2N} \times C_{max1N}/C_{max2N}$.

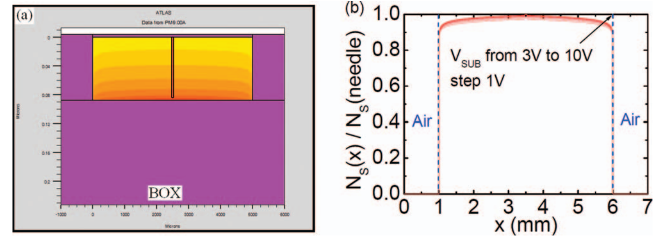


**Figure 11.** (a) Electron concentration simulated by ATLAS taking into account real dimensions of the cell ($T_{Si}$ = 88 nm, $T_{BOX}$ = 145 nm, and $d_{cell}$ = 5 mm) and interface states in borders (Nit = $10^{11}$ cm$^{-2}$). $V_{SUB}$ = 10 V. (b) Ratio between the concentration along the film and the concentration in the needle (at 84 nm depth from the Si surface) for substrate biases from 3 V to 10 V. The doping concentrations for the silicon film and the needle region are per surface unit. It is demonstrated that the results support our assumption since the concentration is almost constant in the large area around the needle at Si film-BOX interface.

In order to complete this study, we analyzed the carrier distribution during the measurements. Once we confirmed that $S_{eff}$ could be considered as a constant value at low frequencies for any value of $V_{SUB}$ higher than the threshold voltage, the carrier density can be calculated as:

$$qNs(V_{SUB}) = Q(V_{SUB})/S_{eff} \quad [11]$$

where $S_{eff}$ was obtained by Eq. 2. Several simulations were performed to evaluate the carrier spreading using the 2-dimensional device solver ATLAS. The structure of an isolated cell of the wafer, as well as the needles, was simulated considering actual dimensions. The cell was surrounded by oxide and interface states were taken into account on the edges for more realistic simulations ($N_{IT} = 10^{11}\ cm^{-2}$). The needles were emulated by highly doped silicon pillars penetrating into the silicon film. This approximation is reasonable for static simulations and guarantees both an ohmic contact and a source of carriers.[9] Figure 11 illustrates the distribution of electron concentration per surface unit, $N_S$, along the Si film at Si-BOX interface considering a one-needle configuration when the substrate bias is modified from $3\ V$ to $10\ V$. The results reveal that the concentration is maximum close to the needle, but drops at the edges as consequence of the border effects. The carrier concentration in the region covered by the effective radius centered in the needle ($2.5\ mm - r_{eff} = 1.1\ mm < x < 2.5\ mm + r_{eff} = 3.9\ mm$) is larger than $95\%$ of the carrier concentration just under the needle and can be considered almost constant. The simulation results verify that our assumption of the constant carrier distribution in the area of $S_{eff}$ is rather reasonable. These experiments indicate the utility of Split-C(V) measurement to determine the carrier density for all $V_{SUB}$ regions where the channel is active in a Pseudo-MOS configuration.

## Conclusions

We have investigated the effective area involved in Split-C(V) measurements with Pseudo-MOSFET. The role of the different parameters (number of the needles and distance between needles) has been clarified. A model to evaluate the effective area has been proposed including the dimensional and measurements conditions of the experimental setup. This model has been validated with several systematic measurements. We also discuss the carrier density determination by using the active area derived from Split-C(V) measurement. Finally, we verified that active area is rather independent of gate bias at low frequencies.

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