Determination of ad hoc deposited charge on bare SOI wafers

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***Abstract*—This work develops an analytical model which correlates the changes of the threshold voltages in Pseudo-MOSFET structures with the charge intentionally placed on the surface of the native oxide. The model has been validated through experimental I-V characteristics obtained when the surface is physically altered with an APTES solution. The measurements were performed in 15 MESA isolated SOI cells. These results open the path for the potential use of the bare SOI wafers as a platform for charge-based sensing applications.**

Keywords—Pseudo-MOSFET, threshold voltage, SOI, charge sensing

I. Introduction

It is well known that, in bare Silicon-On-Insulator (SOI) wafers electrically characterized by point-contact methods, the top surface plays a crucial role on the channel properties through the top density of interface traps (D_{it2} in Figure 1) [1]. The effect of the traps is particularly noticeable when the Silicon film thickness is scaled down to the decananometer range and the coupling between the channel and the surface is strengthen [2]. This impact is amplified for non-passivated surfaces where D_{it2} can reach values over 10^{13} $cm^{-2}eV^{-1}$ [1].

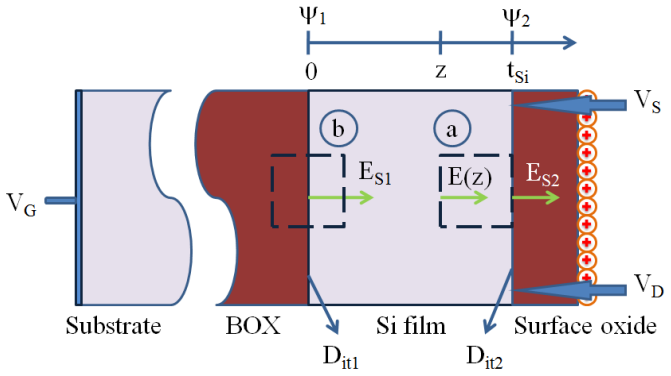

Fig.1. Simplified cross-section of an SOI wafer for two-point contact electrical characterization (Pseudo-MOSFET) technique: V_S is the source voltage, V_D is the drain voltage both applied by pressure adjustable probes. V_G is the gate (substrate) voltage. D_{it1} and D_{it2} represent the density of interface states at BOX-Si film and Si film-top surface interfaces respectively. Two Gaussian surfaces in both edges of the Si film (dashed line, *a* and *b*) are represented.

In contrast, the density of interface states at the Si-BOX interface takes a minor role on the electrical characteristics of the induced channel since D_{it1} is typically well below 5×10^{13} $cm^{-2}eV^{-1}$.

Furthermore, it has been shown by *Ionica et al.* [3] that the ad hoc deposition of charged particles on the free surface of the wafer, influences additionally on the Pseudo-MOSFET electrical parameters by modifying the conduction of the electron or hole channels.

In this work we have derived a theoretical model to calculate the amount of deposited charge on the surface by its impact on the shift of the threshold voltage observed in static I-V curves. This model can be used to establish a closed protocol to correlate the change in electrical parameters with the concentration of a charged solution.

II. Theoretical Model

Firstly, Gauss law was applied to the first closed-surface shown in Figure 1 (noted as surface (a)) in order to establish the boundaries conditions at the top oxide-Si film interface [4]. The continuity of the electrical displacement at $x = t_{Si}$ yields:

$$-\varepsilon_{Si}\left(\partial\psi/\partial x\right)_{x=t_{Si}} = Q_{x=t_{Si}} \qquad (1)$$

where ψ is the electrostatic potential along the z direction. If we assume that traps are uniformly distributed in terms of energy, the associated interface charge can be considered proportional to the potential [5]; the electric field at top oxide-Si film is:

$$E_{S2} = \left(qD_{it2}\psi_{S2} + Q_{SUP}\right)/\varepsilon_{Si} \qquad (2)$$

Q_{SUP} in (2) represents the ad hoc deposited charge (uniformly distributed on the surface) and ψ_{S2} is the potential at the top surface.

Similar conditions were also applied to the surface (b) in Figure 1 (BOX-Si film interface) resulting:

$$\varepsilon_{BOX} E_{BOX} - \varepsilon_{Si} E_{S1} = Q_{x=0} \tag{3}$$

Developing Eq. (3) and assuming a linear drop of the electrostatic potential inside the BOX we obtain:

$$\varepsilon_{BOX} \left(V_G - \phi_{fb} - \psi_{S1} \right) / t_{BOX} - \varepsilon_{Si} E_{S1} = qD_{it1} \psi_{S1} \tag{4}$$

where ϕ_{fb} is the flatband voltage (ϕ_{fb} = 0 in our case since the Si film and the Si substrate below the BOX are equally doped) and ψ_{S1} is the potential at the channel interface.

Lastly, the potential profile inside the Silicon film can be approximated by a linear law for non-passivated samples, since the field tends to be constant across the film [4]:

$$E_{S1} = E_{S2} = (\psi_{S1} - \psi_{S2}) / t_{Si} \tag{5}$$

Combining Eq. (2), (4) and (5) the expression for the threshold voltage of the induced channel accounting for the surface charge is given by Equation (6).

$$V_G = \left\{ \phi_{fb} + \psi_{S1} \left[1 + C_{it1} / C_{BOX} + C_{Si} C_{it2} / C_{BOX} (C_{Si} + C_{it2}) \right] \right\} + \\ + Q_{SUP} \, C_{Si} / C_{BOX} (C_{Si} + C_{it2}) \tag{6}$$

where $C_{BOX} = \varepsilon_{BOX}/t_{BOX}$ is defined as the buried oxide capacitance, $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the Silicon film capacitance, and $C_{it1} = q \cdot D_{it1}$ and $C_{it2} = q \cdot D_{it2}$ are the capacitances associated to traps in each interface of the Si film.

The first term in the second part of the Eq. (6) corresponds with the formula of the threshold voltage in a Pseudo-MOSFET structure [4]. So, for the threshold condition ($\psi_{S1} = 2\phi_F$, $V_G = V_{TH}$) the charge deposited at the surface on the sample can be related to the threshold bias shift (ΔV_{TH}) with respect to the untreated surface by the lowing equation:

$$Q_{SUP} = \Delta V_{TH} \, C_{BOX} (C_{Si} + C_{it2}) / C_{Si} \tag{7}$$

The final expression for Q_{SUP} takes into account not only the thickness of the SOI sample, but also the quality of the top oxide. The densities of states D_{it2} and D_{it1} can be determined experimentally on a previous stage by calibrating Eq. (6) when $Q_{SUP} = 0$ [4].

III. Experimental Results

In order to check the validity of the model, several experiments were carried out depositing a charged solution on the SOI samples and performing Pseudo-MOSFET measurements. The experimental setup consists of a Jandel® probe station with tungsten probes of 25µm tip radius. The distance between the point-contacts was 1.59mm and the pressure was controlled by pressure-adjustable probe arms with integrated dynamometers.

A. Monitorization of the threshold voltage variability

Due to the lack of implanted contacts in Pseudo-MOSFET setup, the measurements performed are very sensitive to the pressure of the needles [6]. An initial calibration of the probe pressure is mandatory to get optimum experimental results.

Additionally, the separation between needles and the cell edges plays an important role in the experimental procedure [7]. These distances are fixed once the sample is situated on the metallic chuck of the probe-station. Nevertheless, successive lifting and dropping of the probes on the surface, creates a large number of defects, which, despite being locally placed, affect the electrical characteristics. Thus, the electrical parameters obtained, such as the threshold voltage, have not a constant value and an averaging must be carried out. To illustrate this effect, Fig. 2 shows an example of 50 consecutive current curves obtained in the same cell of a SOI wafer by a Pseudo-MOSFET setup. As observed, the results show an unavoidable variability due to consecutive measurements.

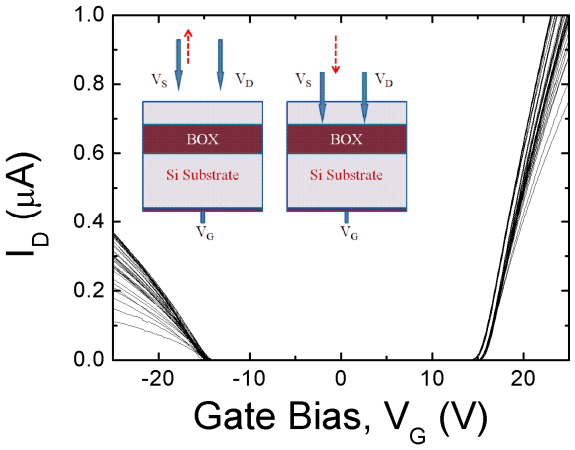

Fig. 2. Example of fifty consecutive current characteristics obtained for the same sample. The measurements are carried out lifting the needles after a measurement and placing them back on the surface of the cell to take a new measurement. Large apparent variability is observed in the transconductance, whereas this variability is much lower in the threshold voltage. t_{Si} = 12nm, t_{BOX} = 145nm, non-passivated wafer.

Fig. 3 represents the threshold voltage values extracted for two cells (Right-hand side: electron channel; Left-hand side: hole channel). The variance of the distribution is also cell dependent as illustrated in Fig. 3 with the results of cell #2. If this variability is too large, the cell is discarded for the experiments since the huge disparity between results may lead to inaccurate Q_{SUP} determination.

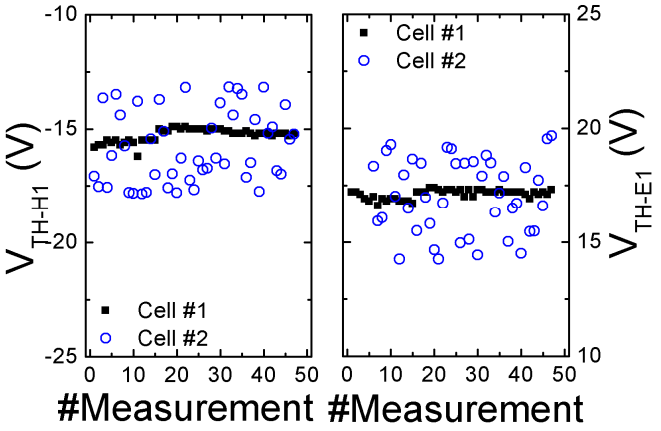

Fig. 3. Threshold voltages extracted from two SOI cells (*Cell #1* corresponds to the cells measured in Figure 2: solid square symbols). LHS: hole-channel, RHS: electron channel). t_{Si} = 12nm, t_{BOX} = 145nm, non-passivated wafer.

B. Extraction of the Q_{SUP} by ad-hoc charge deposition

We studied 15 cells of a non-passivated SOI sample (INSET of Fig. 4) with 12nm-thick Si film and 145nm-thick BOX. Because of the ultrathin Si film, the ad-hoc charge will have a stronger influence on the channel electrical characteristics leading to a noticeable shift in $I_D(V_G)$ curve. The experimental methodology followed was:

1) Calibration of the probe pressure was done on first stage. Current curves were obtained when pressure is varied from *10gr* to *100gr*. At *80gr* the transconductance peak (obtained as the derivative of the current, $\partial I_D/\partial V_G$) saturates and this pressure was established as the optimum.

2) All the cells involved in the study were characterized as detailed in Section A to extract the threshold voltage reference values.

3) Then, the sample was introduced into a 2% solution of Amino-Propyl-Tri-Ethoxy-Silane (APTES) [8] diluted in acetone for *30s*. Next, it was cleaned with distilled water and left into a class-10 clean cabin for 24 hours.

4) Finally the threshold voltage is extracted again, and the value of Q_{SUP} is calculated from the model (Eq. (7)). Both hole and electron channels are probed taking the statistical mean of threshold voltages for the 15 cells.

Fig. 4 shows an example of the voltage shift observed in the current characteristics obtained for one of the SOI cells. The APTES treatment creates an amino-terminated layer on the surface which is positively charged [8]. It increases the electrostatic potential inducing negative charge below the surface oxide (capacitive coupling). The film inversion is favored (the threshold voltage for electrons decreases) whereas the film accumulation is lessened (residually doped p-type wafer). The average values of V_{TH-H} and V_{TH-E} were monitored for the fifteen as-fabricated cells (reference) and the cells after the APTES deposition. Results are shown in Fig. 5.

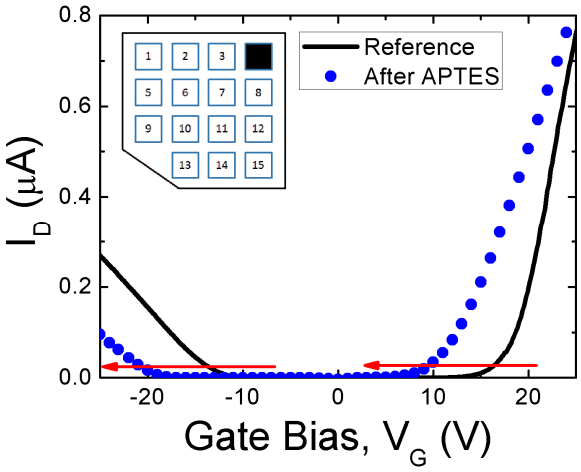

Fig. 4. When a positive charged layer is added on the wafer surface, a shift of the current curves is produced (pointed by the arrows). The gate bias, V_G, was modified from -25V to 25V and the sweep total time was approximately 60s. INSET: Schematic of the sample containing the MESA isolated SOI cells.

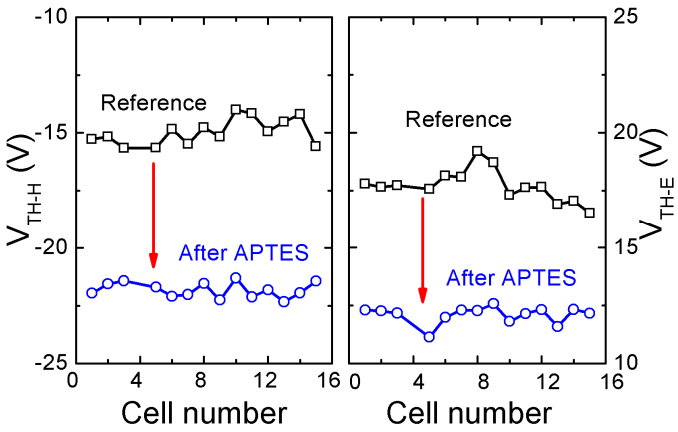

Fig. 5. Threshold voltages for hole (left) and electron (right) channels extracted from the $I_D(V_G)$ curves before (squares) and after (circles) the APTES layer is created on the native oxide of the cells. 15 cells are probed.

To conclude, Table 1 summarizes the absolute value of the extracted surface charge Q_{SUP} by applying Eq. (7) from the average values of Fig. 5. The value of D_{it2} was calibrated from the models in [5] using $D_{it1} = 2 \cdot 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ (obtained for non-passivated samples).

Hole channel	**Reference**	**After APTES**
$<V_{TH-H}>$ (V)	-15.38	-22.25
$<D_{it2-H}>$ ($cm^{-2}eV^{-1}$)	$1.47 \cdot 10^{13}$	$1.47 \cdot 10^{13}$
Q_{SUP} (C/cm^2)	-	$3.32 \cdot 10^{-6}$
Electron channel	**Reference**	**After APTES**
$<V_{TH-E}>$ (V)	17.02	12.11
$<D_{it2-E}>$ ($cm^{-2}eV^{-1}$)	$2.37 \cdot 10^{13}$	$2.37 \cdot 10^{13}$
Q_{SUP} (C/cm^2)	-	$3.76 \cdot 10^{-6}$

Table 1. Set of data employed to extract Q_{SUP} through the model given by Eq. (7). The different intermediate parameters extracted for hole and electron channel are presented.

The agreement between the values of Q_{SUP} extracted for hole and electron channels demonstrate the usefulness of the model to evaluate charge deposited on the surface of the wafer and measured by a simple point-contact method.

IV. Conclusions

This works presents a theoretical model to obtain the surface charge in a Pseudo-transistor when a certain charge solution is intentionally deposited on the bare surface. The threshold voltage shift is reported after deposition. The model is based on Gauss law applied to both interfaces of the Silicon film and its accuracy has been tested over several SOI samples. The results point the Pseudo-MOSFET technique as a potential and simple platform for sensing applications.

Acknowledgements

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