Effective Mobility in Extra-Thin Film and Ultra-Thin BOX SOI Wafers

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1. Abstract

This paper proves that the pseudo-MOSFET is still a very successful characterization technique for bare SOI even when the film and BOX thicknesses are dramatically reduced. We demonstrate for the first time the ability to characterize extra-thin SOI structures down to 12 nm silicon film and 25 nm BOX with two different methods using the pseudo-MOSFET configuration. Effective mobility curves were extracted from static drain current curves and compared with those from split *C-V* measurements for validation. The impact of surface passivation is also discussed.

2. Introduction

The transport properties of as-grown fully depleted SOI films are unveiled by the pseudo-MOSFET (Ψ-MOSFET, Fig. 1a) technique before completing the CMOS process [1]. The Ψ-MOSFET contributes to the optimization of SOI technologies by providing valuable information on basic wafer electrical parameters.

In our previous work [2], we demonstrated the possibility to extend the Ψ-MOSFET configuration to split *C-V* measurements and to obtain the effective mobility (μ_{eff}). We now confirm this capability: (i) by characterizing SOI wafers with 12 nm extra-thin film (ETF) and 25 nm ultra-thin buried oxide (BOX) and (ii) by evaluating the effective mobility curves obtained by two different measurements techniques. Wafers with and without surface passivation have been compared.

3. Split *C-V* measurement

The split *C-V* method [2] is based on the channel-to-gate capacitance C_{gc} measurement as a function of the gate voltage V_g for a frequency range from 40 Hz to 1 kHz. The back-gate is biased and the source and drain pressure probes are connected to the ground (Fig. 1b). The integral of the *C-V* curve yields the inversion/accumulation charge density. The effective mobility, function of electric field, or V_g, is determined from the corresponding value of the drain current.

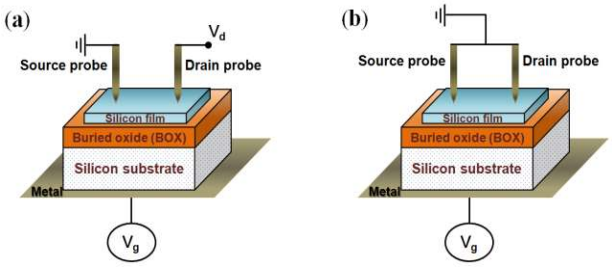

Fig. 1: *Schematic configuration for Ψ-MOSFET (a) current and (b) split C-V measurements.*

4. Results and discussions

In extra-thin Si layer and BOX the probability to damage the BOX by the probe penetration and to have current leakage is very high. By carefully adjusting the pressure on the probes, we succeeded to obtain reproducible Ψ-MOSFET characteristics. The drain current (I_d) and transconductance (g_m) curves *versus* V_g are shown in Fig. 2. No current leakage is visible. The coupling of the buried channel with the free surface defects is very strong in ETF SOI [3]. The impact of this coupling was studied by measuring and comparing passivated (with 4 nm oxide layer on the film surface) and non-passivated samples (Fig. 2).

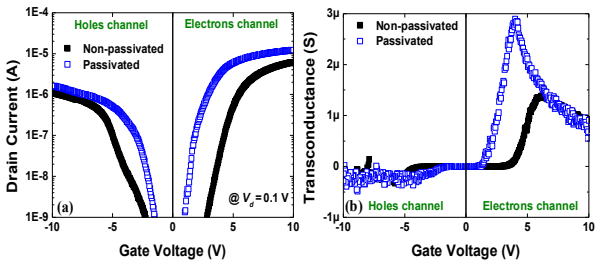

Fig. 2: *(a) I_d vs. V_g and (b) g_m vs. V_g for SOI wafer with 12 nm Si film (passivated and non-passivated) and 25 nm BOX. Probe pressure is 15 g.*

$I_d(V_g)$ curves show lower threshold voltage V_t and swing S in the passivated samples than in non-passivated ones. This is a direct consequence of the reduction in the defect density at the wafer surface ([3], [4]). The $g_m(V_g)$ curve for passivated samples shows a

large increase of the peak and therefore of the field-effect mobility.

The curve behaviour is not similar for electrons and holes in both Ψ-MOSFET and split *C-V* measurements. This is due to the high impact of series resistance (R_{sd}) [5] and/or to the possible depletion underneath the BOX on holes side (for negative V_g). We will focus on the inversion side of the curves (electron channel).

Fig. 3 shows split *C-V* measurements obtained on the same wafers. Both electron and hole channels are activated. A maximum value of the capacitance (Fig. 3) corresponding to the BOX capacitance is obtained at high positive and negative voltages. Fig. 3 also shows the dependence of the *C-V* curves on frequency for non-passivated wafer. As the frequency increases, the *C-V* curves are shifted to a higher threshold voltage and the maximum capacitance decreases.

These effects are related to the time response of electrons needed to activate the channel between source and drain. The *C-V* curves of passivated surface sample (not shown here) indicate a lower V_t compared to the non-passivated sample. These results confirm those deduced from Ψ-MOSFET $I_d(V_g)$ curves.

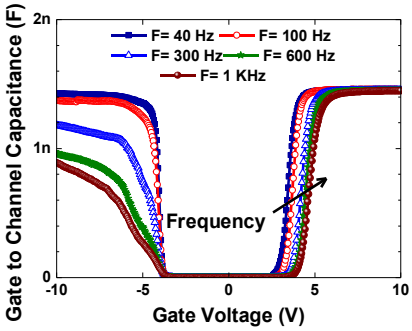

Fig. 3: *C_{gc} vs. V_g for various frequencies. 12 nm non-passivated Si film and 25 nm BOX.*

The effective mobility for electrons μ_{eff} which characterizes the transport at the Si-BOX interface is calculated by two methods: (i) conventional $I_d(V_g)$-based extraction method by the *Y*-function [6] and (ii) adapted split *C-V* technique detailed in [2]. The key difference between these two methods is that μ_{eff} evaluated from static measurements is reconstructed by calculating the inversion charge $Q_{inv}(V_g)$. However for split *C-V*, μ_{eff} is directly measured by integrating the capacitance (C_{gc}) over the selected V_g range.

The electron effective mobility *versus* gate voltage in SOI samples, calculated with both methods, are illustrated in Fig. 4a for non-passivated sample and in Fig. 4b for passivated sample. The mobility curves from static and split *C-V* match together and superpose in strong inversion. These experimental results confirm the feasibility and efficiency of Ψ-MOSFET split *C-V* technique to characterize ultra-thin SOI structures.

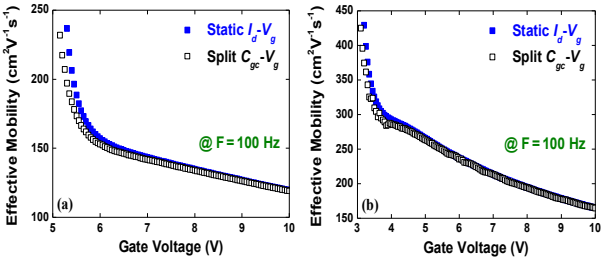

Fig. 4: *Electron effective mobility μ_{eff} as a function of V_g (for $V_g > V_t$) calculated from static $I_d(V_g)$ and split C-V curves on (a) non-passivated and (b) passivated SOI samples.*

Fig. 5 shows μ_{eff} plotted *versus* V_g for passivated (empty squares) and non-passivated (solid squares) surfaces. The split *C-V* method clearly confirms that passivated sample offers better mobility (up to 30 %) compared to the non-passivated one in agreement with ([3], [4]). But their figure of merit is to be obtained for the first time on such thin film/BOX couple.

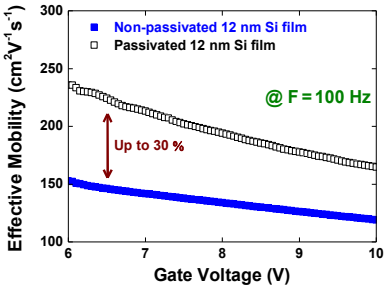

Fig. 5: *Electron μ_{eff} as a function of V_g calculated from split C-V curves for passivated and non-passivated Si film.*

5. Conclusions

In conclusion, we demonstrated the capability of exploring very thin as-fabricated SOI wafers using the pseudo-MOSFET and the adapted split *C-V* technique. We showed the electron effective mobility curves in 12 nm extra-thin Si-film and 25 nm ultra-thin BOX. Excellent agreement was obtained between the results determined from static and *C-V* measurements. Passivated samples showed higher mobility values than non-passivated ones.

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References

[1] S. Cristoloveanu *et al.*, IEEE TED **47**, 1018 (2000).
[2] A. Diab *et al.*, Proc. of EuroSOI conference, 103 (2012).
[3] G. Hamaide *et al.*, J. Appl. Phys. **101**, 114513 (2007).
[4] N. Rodriguez *et al.*, IEEE TED **56**, 1507 (2009).
[5] I. Ionica *et al.*, Appl. Phys. Lett. **94**, 012111 (2009).
[6] G. Ghibaudo, Electronics Lett. **24**, 543 (1988).