Substrate effect on Pseudo-MOSFETs capacitance curves

Cristina Fernandez Sanchez, Departamento de Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, Spain, email: cfsanchez@ugr.es
Noel Rodriguez Santiago, Departamento de Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, Spain, email: noel@ugr.es
Francisco Gámiz Pérez, Departamento de Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, Spain, email: fgamiz@ugr.es

Abstract

The Pseudo-MOSFET technique has been used during decades for the monitoring of unprocessed Silicon-On-Insulator (SOI) wafers. Until now, this characterization method had been only used for the extraction of electrical parameters from DC results. Recently, the Pseudo-MOSFET was combined with AC measurements through Split-CV technique. This allowed to extract capacitance curves varying the gate bias applied, and to study the frequency dependence of the structure. Nevertheless, there exist several aspects not yet studied.

In this work, the effect of the gate bias on capacitance measurements is analyzed in terms of the variability of the depletion region thickness under the BOX. To do this, a theoretical model will be proposed and discussed with experimental results obtained in laboratory. Finally, for the purpose of benchmarking, the study will be carry out for various wafers with different layer thicknesses.

Keywords

Silicon-on-Insulator (SOI), Pseudo-MOSFET, Split-C(V), substrate thickness, effective area

1 Introduction

The Pseudo-MOSFET technique is a well-established simple method for the electrical characterization of bare Silicon-On-Insulator (SOI) wafers. The method takes advantage of the MOSFET-like configuration implicit in any SOI wafer (Fig. 1.a)) [1][2]: the substrate serves as the gate terminal, the Buried-Oxide (BOX) plays the role of the gate insulator, and the Silicon film acts as the transistor body. For the source and drain contacts two metallic needles are placed on the wafer surface. Thus, when a gate bias is applied, a channel can be induced in the film and current curves can be extracted.

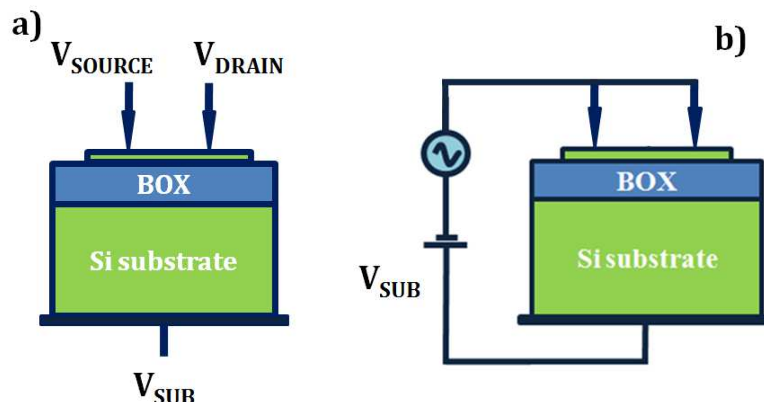

Figure 1: a) usual Pseudo-MOSFET configuration, b) double-needle capacitance experiment.

Recently, this method has been combined with Split-C(V) measurements (Fig 1.b)). Split-C(V) technique enables to obtain the inversion or accumulation charge in a MOSFET, Q_i, integrating the direct measurement of the gate-to-channel capacitance, C_{GC}, [3].

One of the most recent research of this double characterization (DC and AC) was the determination and modeled of the effective surface, S_{eff} [4]. This effective area represents the maximum region around the needles where the carriers (electrons or holes) are able to follow the AC input signal (Fig 1.a)). The present work uses these previous and reported results in a deeper study of the frequency dependence of the Pseudo-MOSFET capacitance curves where the substrate thickness makes its appearance on the scene.

1.1 Pseudo-MOSFET as a capacitor

When AC measurements are performed, the Pseudo-MOS transistor can be modeled as a set of planar capacitors. A simple approximation is the sum of the capacitance associated to the BOX, and that formed by the depletion region under the BOX (Fig 1.a)). Unlike the BOX capacitance, the second capacitor is only created when the frequency is high enough. The reason comes from the coefficient diffusion of electrons and holes. At higher frequencies, the diffusion of carriers is limited and those far from the needles are not able to follow the AC signal, generating a depletion region [5].

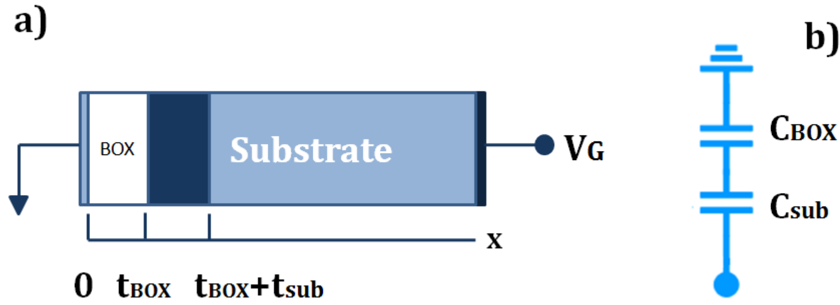

Figure 2: a) when the frequency is high enough a depletion region in the substrate appears, b) electrical circuit equivalent

1.2 Substrate thickness

The electrical circuit associated to this approach is shown in Fig. 2.b): two capacitors in series form the Pseudo-MOS transistor. From this scheme, the theoretical total capacitance can be represented as:

$$\frac{1}{C_T} = \frac{1}{C_{BOX}} + \frac{1}{C_{sub}} \quad [1]$$

Whether the capacitances are treated as planar capacitors, the substrate depletion thickness can be extracted:

$$\frac{1}{C_T} = \frac{t_{BOX}}{S_{eff}\varepsilon_{BOX}} + \frac{t_{sub}}{S_{eff}\varepsilon_{sub}} \quad [2]$$

$$t_{sub} = \varepsilon_{sub}\left(\frac{S_{eff}}{C_T} - \frac{t_{BOX}}{\varepsilon_{BOX}}\right) \quad [3]$$

The dielectric constants ε_{BOX} and ε_{Si} are those associated to the SiO_2 buried oxide and the Silicon substrate. The maximum value of capacitance, C_T, is obtained from experimental curves at strong inversion or accumulation depending on the gate terminal value: at high positive values electrons determined the capacitance value, and at high negative gate biases will be the holes. Finally, the effective area, S_{eff}, has been reported being possible to calculate its value for any frequency [4]. Therefore, t_{sub} can be extracted as a function of the frequency.

2 Materials and Methods

To carry out the calculations, capacitance curves were performed employing some material of the Nanotechnology Laboratory placed in CITIC (University of Granada). In particular, it was necessary to use the Jandel probe station where the samples are placed and biased though the metallic chuck and the needles (Fig. 3).

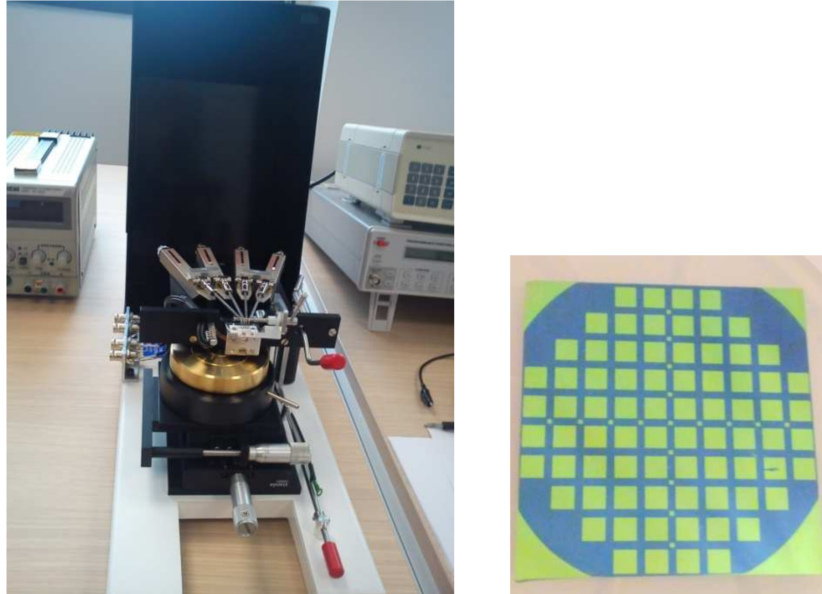

Figure 3, Jandel probe station and the Pseudo-MOS sample used

Furthermore, an impedance analyzer as well as various cables and connectors were utilized (Fig. 4). The analyzer allows us to modified the frequency of the input signal as well as the bias of the substrate (chuck in the probe station).

Figure 4: Impedance analyzer and connectors used to extract capacitance curves from the Pseudo-MOSFET samples.

3 Results and discussion

3.1 Capacitance curves and effective area

Capacitance measurements varying the frequency of the signal were performed on a non-passivated [6] Pseudo-MOSFET sample with 145nm-thick BOX and 88nm-thick Si film. In order to explore and compare several results two configurations were studied: using one needle on the surface and two. The curves extracted are represented in Fig. 5.

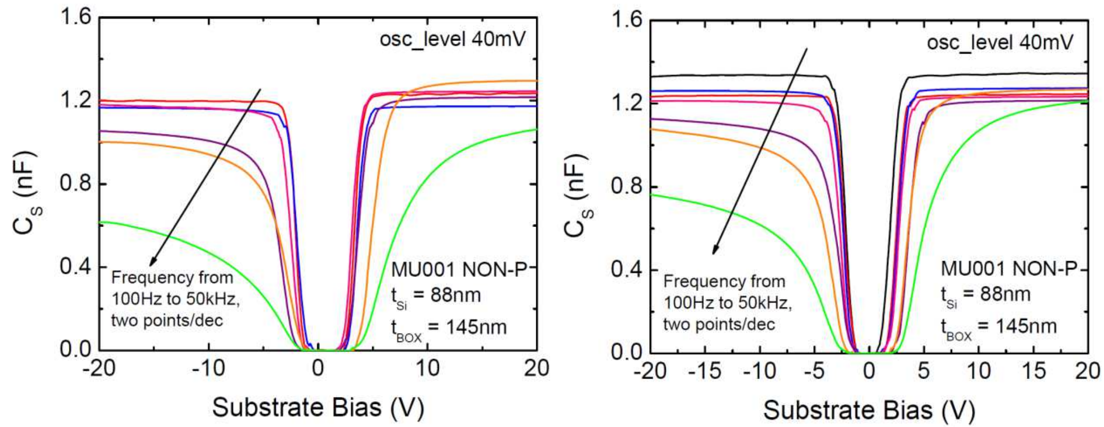

Figure 5. Capacitance curves obtained using one needle on the Pseudo-MOSFET surface (left) and two probes (right).

After extracting the maximum value of the curves (C_T) for both electrons and hole channels (using a substrate bias positive and negative respectively) the effective area was calculated from [4]. The results for these curves are depicted in Figure 6. As observed, the area remains as a constant at low frequencies, which indicates that carriers are still able to follow the AC signal. Nevertheless, for higher frequencies they are limited and S_{eff} decreases.

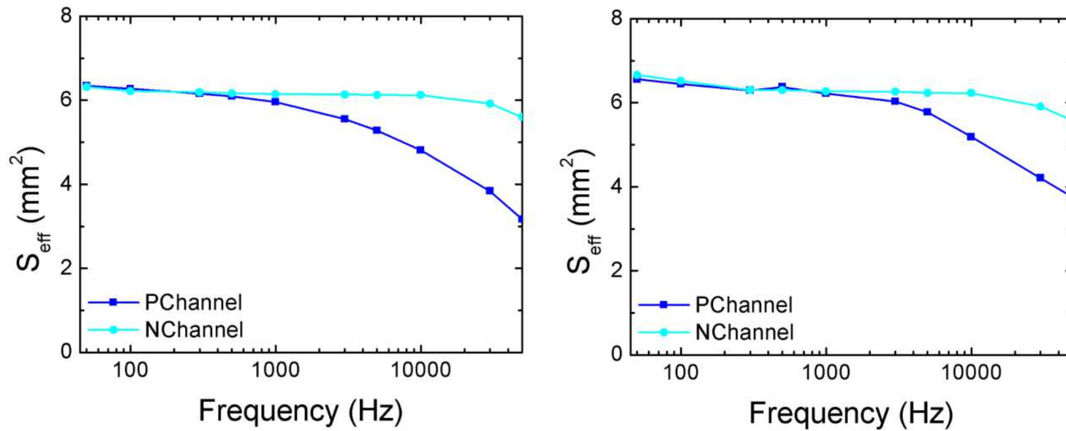

Figure 6. Effective area obtained from [3] using the capacitance curves extracted in our experiment for one needle on the surface (left) and two (rigth).

3.2 Substrate thickness

To complete the study, the substrate thickness associated with the depletion region at high frequencies was calculated by Eq. [3] (Fig. 7). The data demonstrate that t_{Sub} begins to increase with the frequency. The results are those expected since when the frequency increases so does the region t_{sub}.

4 Conclusions

Since its invention, the Pseudo-MOSFET has been used for the characterization and optimization of SOI wafers. Its current curves are similar to those for an usual MOSFET, being possible to employ the same parameter extraction methods to determine the material parameters.

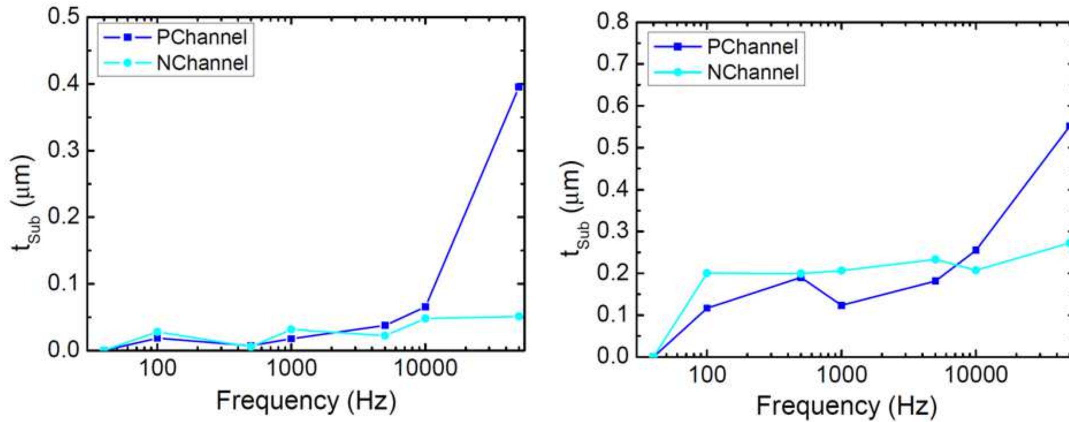

Figure 7. Substrate thickness values obtained as a function of the frequency employing one needle on the surface (left) and two (rigth).

Recently, this characterization has been expanded to a capacitance analysis through the Split-C(V) technique. In this work, the behavior of the transistor with respect to the frequency of the AC input signal has been further studied. In particular, how the thickness of the depleted region under the BOX has been analyzed. Capacitance measurements were carried out using lab material and the area effective from the curves was calculated. The results satisfied our hypothesis about the carriers: since carriers are not able to diffuse when the frequency is high, the depleted zone increases its thickness.

5 References

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